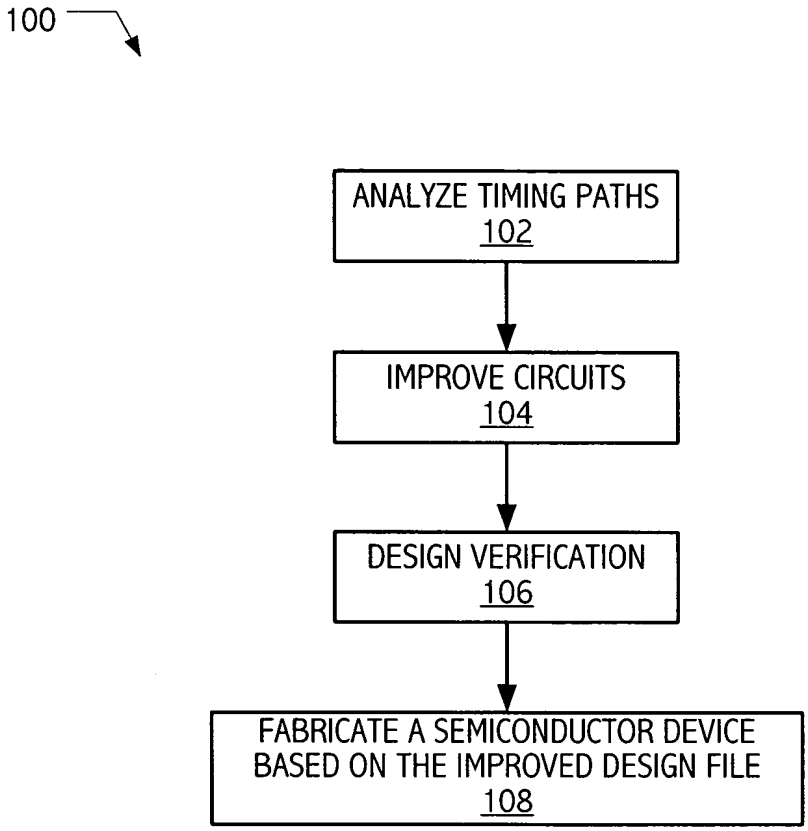
100
ANALYZE TIMING PATHS
102
IMPROVE CIRCUITS
104
DESIGN VERIFICATION
106
FABRICATE A SEMICONDUCTOR DEVICE
BASED ON THE IMPROVED DESIGN FILE
108

FIG. 1

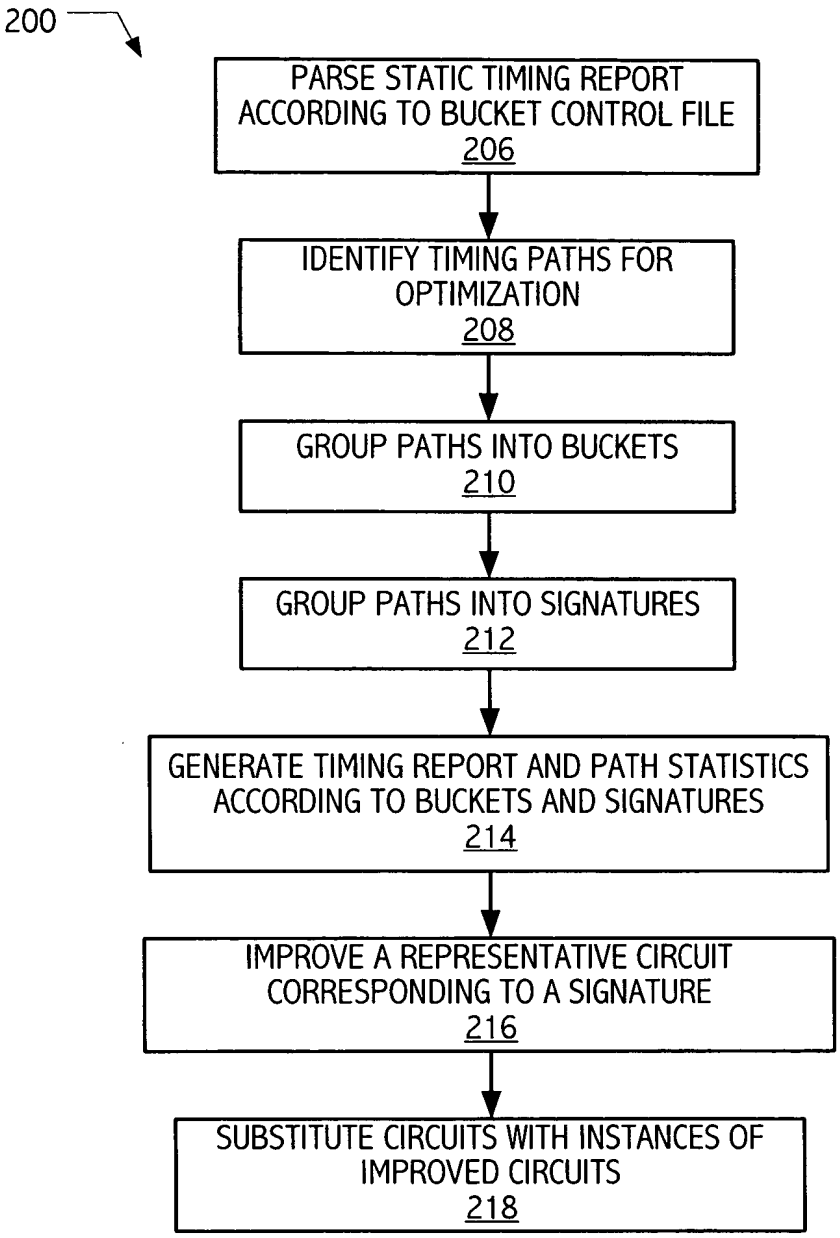
200
PARSE STATIC TIMING REPORT ACCORDING TO BUCKET CONTROL FILE
206
IDENTIFY TIMING PATHS FOR OPTIMIZATION
208
GROUP PATHS INTO BUCKETS
210
GROUP PATHS INTO SIGNATURES
212
GENERATE TIMING REPORT AND PATH STATISTICS ACCORDING TO BUCKETS AND SIGNATURES
214
IMPROVE A REPRESENTATIVE CIRCUIT CORRESPONDING TO A SIGNATURE
216
SUBSTITUTE CIRCUITS WITH INSTANCES OF IMPROVED CIRCUITS
218

FIG. 2

302

(1) Bucket by source block name:

BUCKET: emcu_ecu_ecaddr_ctl
PRIORITY: 43
SOURCE: emcu_ecu_ecaddr_ctl ←bucket by source block
DESTINATION:
NET:
DEVICE:

304

(2) Bucket by destination block name:

BUCKET: emcu_ecu_ecaddr_dp
PRIORITY: 45
SOURCE:
DESTINATION: emcu_ecu_ecaddr_dp ←bucket by destination block
NET:
DEVICE:

306

(3) Bucket by source block name:

BUCKET: ramtest
PRIORITY: 100
SOURCE:
DESTINATION:
NET: ramtest ← bucket by common net name (useful for bus)
DEVICE:

308

(4) Bucket by device name:

BUCKET: emu_ecu_ecaddr_dp
PRIORITY: 45
SOURCE:
DESTINATION:
NET:
DEVICE: paths_share_common_device ← bucket by common device

310

(5) Bucket by combination of fields:

BUCKET: ramtest
PRIORITY: 100
SOURCE: ramtest
DESTINATION: ramtest
NET: ramtest
DEVICE: ramtest

FIG. 3

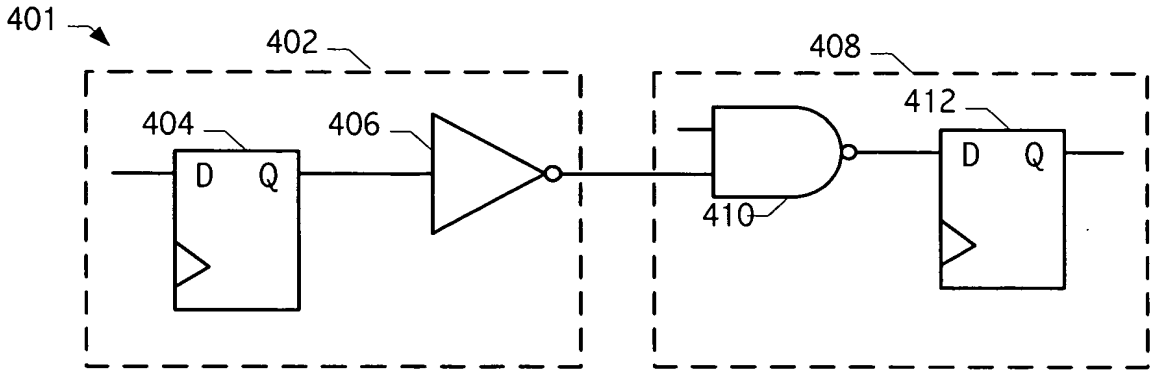

FIG. 4A

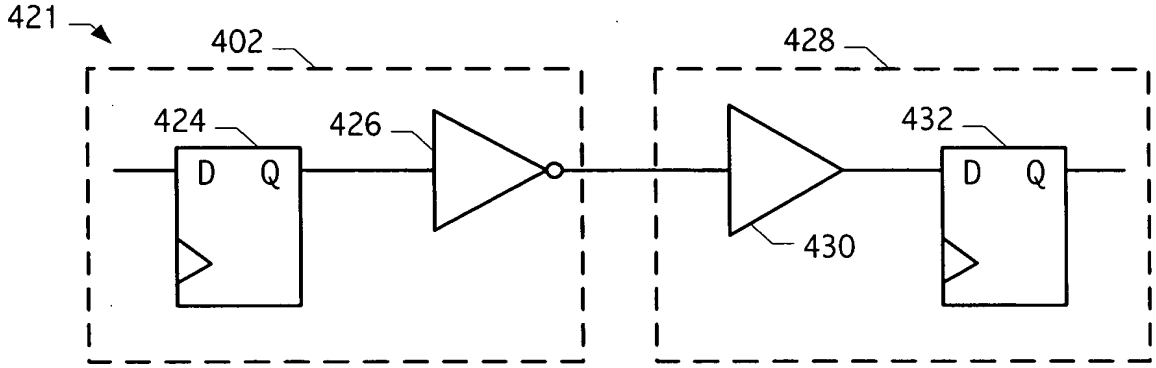

FIG. 4B

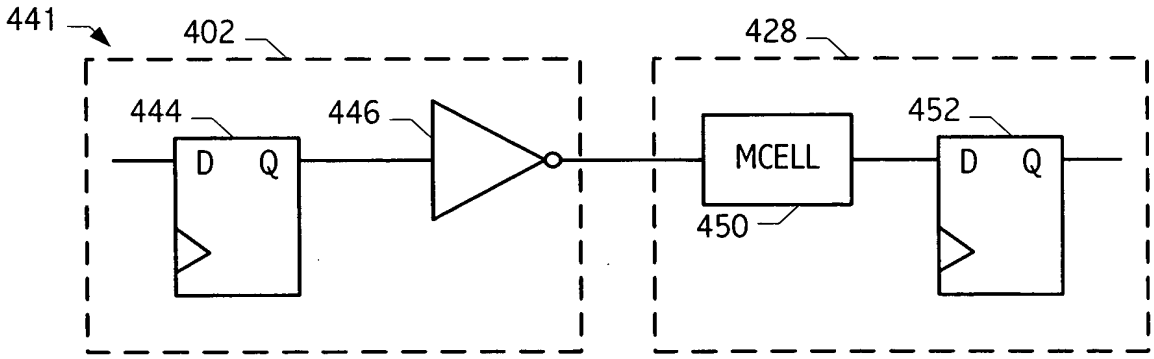

FIG. 4C

MAX T = 0.974ns : 30 paths : 3 signatures : BUCKET 1_AAA
MAX T = 0.957ns : 6 paths : 1 signatures : BUCKET 2_BBB
==========
<1__emu>

1 : BUCKET: AAA
PRIORITY: 45
SOURCE:
DESTINATION:
NET: aaa
DEVICE:

Number of paths = 30

Number of signatures = 2

signature # 1 : ecram.mux4i.inv.eccgen.fsdsql
bucket : 1_AAA
p1(0.974ns) p2 (0.971ns) p6(0.967ns) p7(0.967ns)

Possibility 1:
Setup constraint violation 0.024ns dev_6 (fsdsql_24x d v -> 12 clk ^)
Clk edge: clk ^ -> dev_6/12clk ^ at 0.000ns +Tcycle = 0.950ns
Clock jitter: 0.100ns
Setup time: -0.120ns
Data dege: clk ^ -> dev_6/d[1] v at 0.994ns
Required cycle time: 0.974ns (1.00 cycle path)

	Delay	Gate	Wire	Load Cap	Node	Device	Cell	Pin to Pin
	0.000ns	0.000ns	0.000ns	560.236pF	clk ^			
*	0.000ns	0.582ns	0.000ns	0.027pF	clk ^	dev_1	ecram	clk ^ → do ^
	0.582ns	0.000ns	0.001ns	0.027pF	aaa ^			
	0.584ns	0.048ns	0.000ns	0.021pF	aaa ^	dev_2	rptr_48x	in ^ → out ^
	0.632ns	0.000ns	0.040ns	0.021pF	bbb ^			
*	0.672ns	0.061ns	0.000ns	0.036pF	bbb ^	dev_3	mux4i_8x	d2 ^ → out v
	0.732ns	0.000ns	0.001ns	0.036pF	ccc v			
	0.733ns	0.036ns	0.000ns	0.151pF	ccc v	dev_4	inv_24x	in v → out ^
	0.770ns	0.000ns	0.022ns	0.151pF	ddd ^			
	0.792ns	0.202ns	0.000ns	0.003pF	ddd ^	dev_5	eccgen	chk ^ → ec v
	0.993ns	0.000ns	0.000ns	0.003pF	eee v			
	0.994ns				eee v			

FIG. 5A

signature # 2 : ecram.mux4i.inv.eccgen
bucket : 1_AAA
p3(0.969ps) p4(0.967ns) p5(0.967ns) p8(0.966ns) p9(0.965ns) p10(0.965ns)
p11(0.959ns) p12(0.958ns) p13(0.958ns) p16(0.957ns) p17(0.956ns) p20(0.956ns)
p21(0.956ns) p22(0.956ns) p23(0.955ns) p26(0.954ns) p27(0.954ns) p28(0.953ns)
p29(0.952ns) p30(0.952ns) p31(0.952ns) p32(0.952ns) p33(0.952ns) p34(0.952ns)
p35(0.950ns) p36(0.950ns)

Possibility 3:
Setup constraint violation 0.019ns dev_5 (eccgen check[3] ^ -> clk ^)
Clk edge: clk ^ -> dev_5/clk ^ at 0.000ns + Tcycle = 0.950ns
Clock jitter: 0.100ns
Setup time: 0.078ns
Data edge: clk ^ -> dev_5/check[3] ^ at 0.792ns
Required cycle time: 0.969ns (1:00 cycle path)

	Delay	Gate	Wire	Load Cap	Node	Device	Cell	Pin to Pin
	0.000ns	0.000ns	0.000ns	560.236pF	clk ^			
*	0.000ns	0.582ns	0.000ns	0.027pF	clk ^	dev_1	ecram	clk ^ → do ^
	0.582ns	0.000ns	0.001ns	0.027pF	aaa ^			
	0.584ns	0.048ns	0.000ns	0.021pF	aaa ^	dev_2	rptr_48x	in ^ → out ^
	0.632ns	0.000ns	0.040ns	0.021pF	bbb ^			
*	0.672ns	0.061ns	0.000ns	0.036pF	bbb ^	dev_3	mux4i_8x	d2 ^ → out v
	0.732ns	0.000ns	0.001ns	0.036pF	ccc v			
	0.733ns	0.036ns	0.000ns	0.151pF	ccc v	dev_4	inv_24x	in v → out
	0.770ns	0.000ns	0.022ns	0.151pF	ddd ^			
	0.792ns				ddd ^			

FIG. 5B

MAX T =	0.847ns :	29 paths :	5 signatures :	BUCKET 1_AAA
MAX T =	0.842ns :	2 paths :	1 signatures :	BUCKET 2_BBB
MAX T =	0.841ns :	138 paths :	3 signatures :	BUCKET 3_CCC
MAX T =	0.840ns :	134 paths :	5 signatures :	BUCKET 4_DDD
MAX T =	0.839ns :	18 paths :	7 signatures :	BUCKET 5_EEE
MAX T =	0.830ns :	3 paths :	2 signatures :	BUCKET 6_FFF
MAX T =	0.824ns :	2 paths :	1 signatures :	BUCKET 7_GGG

FIG. 6